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A Low Power, Low Noise Heart Variability Sensor Design

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A Low Power, Low Noise Heart Variability Sensor Design

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REPORT

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A Low Power, Low Noise Heart Variability Sensor Design

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The University of Texas at Austin, 2013

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This project shows a design for a low power and low noise analog front end for a heart variability sensor. Chopper Stabilization is a well known technique for reducing noise of an amplifier and is used to reduce the noise in the Instrumentation Amplifier in this project. A d/dt peak detector is used to find the peaks of the heart beats. Low power, low noise heart variability sensors can look for patterns in a patient's heart beat which can be correlated to known patterns for certain diseases. This can help doctors determine a patient's susceptibility to these disease and prescribe preventitive treatment in advance.

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Chapter 1

Introduction

1.1 Motivation

Heart rate variability (HRV) is the variation in time between the peaks of a person's heart beat. It has been found that reduced HRV can be a predictor of a variety of diseases. Reduced HRV has been found in patients following a heart attack. Low HRV has been found in patients with diabetes that led to degradation of nerves that control blood pressure and other automatic functions of the brain. Patients who have suffered from cardiac failure have also shown reduced HRV. Low HRV has also been linked to high stress and also to patients with Post Traumatic Stress Disorder (PTSD). There are a number of ways to measure HRV, but ECG is the most popular. Time domain analysis of the HRV is based on statistically analyzing the time difference of successive R-R peaks in the QRS complex.

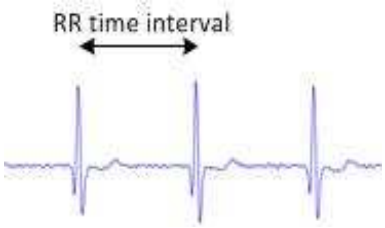

Figure 1.1: R-R peaks in a QRS complex

Analyzing them requires a large sample of peaks taken over a long period of time. It is therefore desirable to have a sensor measure the peaks over long periods of time without having to be attached to a power source so that the patient can take measurements while performing normal day to day activities. This sensor must also be small enough to be wearable by the patient. Interest has been gaining in developing wearable, low power, and wireless biomedical sensors. These sensors allow data about a patient to be taken over long periods of time allowing doctors to make better more informed diagnosis. Thay also allow for in-home patient care allowing for patients to be monitored while going about their daily lives. This reduction in hospital visits helps reduce medical costs. This paper demonstrates a low power, low noise AFE for measuring peaks in a person's heart beat for measuring heart rate variability. The focus will be to make the AFE as low power and low noise as possible. This front end is intended for a wireless wearable sensor.

1.2 Paper Organization

The paper is organized as follows.

Chapter 2 will look at the theory of chopper stabilized amplifiers and discuss signal modulation and noise. It will also look at wet and dry electrodes.

Chapter 3 will discuss the overall architecture of this sensor and challenges that will need to be solved.

Chapter 4 will go over the design in detail.

Chapter 5 will look at the simulated results

Chapter 6 will contain the conclusion and discuss future work.

Chapter 2

Principles

2.1 Context

A full heart variability system will have electrodes that sense the ECG signals connected to the sensor's AFE. The signal will be amplified while minimising noise and the peaks are detected and stored in memory. Doctors can then upload the peak information wirelessly for analysis.

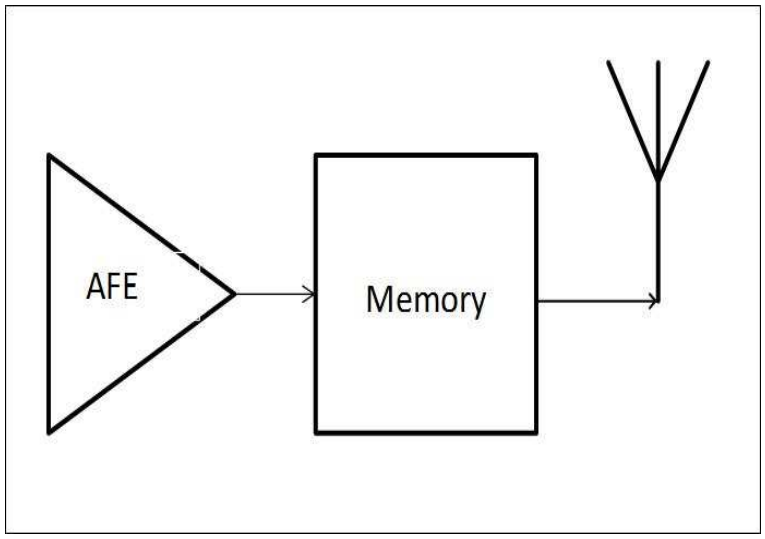

Figure 2.1: Heart Variability Sensor

The sensor must be careful to account for several noise sources common in

ECG sensors. It must account for interference from nearby power lines which occur at 50Hz or 60Hz plus their harmonics. ECG sensors also suffer from DC noise resulting from patient movement, muscle contraction, and the movement of the chest due to respiration and will need to be high pass filtered. The frequency range of the input into the AFE is 0.4Hz to 40Hz. The AFE must support an input dynamic range of 10mV p-p and it's input impedance must exceed 5M Ω. It must also tolerate an input electrode impedance imbalance of 620kohms|| 4.7nF and 51Kohms|| 47nF. System nosise must not exeeced 30uV p-p.

The AFE consists of an Instrumentation Amplfiier, a Low Pass Filter, and a Peak Detector.

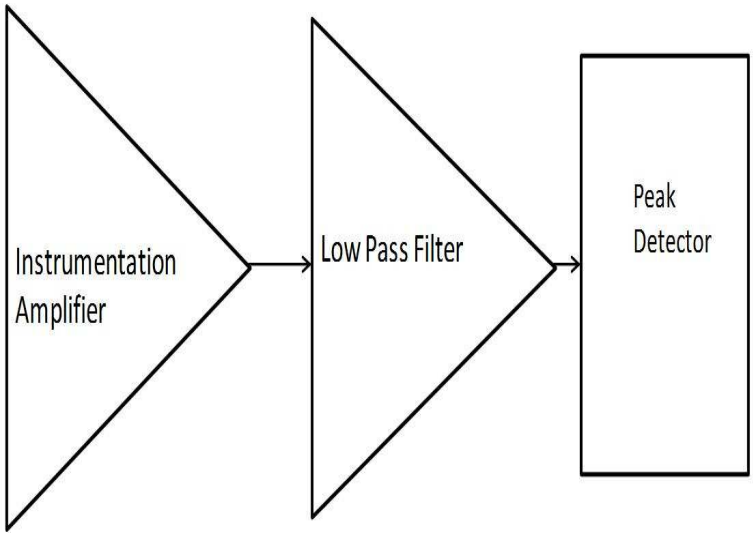

Figure 2.2: AFE

The Instrumentation Amplifier amplfies the incoming signal and establishes the high pass corner at 0.4Hz. A low pass filter is used to set the low pass corner at

40Hz. The output feeds a peak detector which looks for the peaks.

2.2 Noise

In the real world sensors must deal with a number of noise sources. The main noise sources of the Instrumentation Amplifier are Electrode offset voltage, thermal noise, and 1/f noise.

Electrical offset voltage can arise from the accumulation of charge on the electrode interface due the interface's capacitance. It can also come from patient movement changing the capacitance of the interface. Therefore the sensor must reject all DC offset noise.

Thermal noise is due to random themal motion of electrons and does not depend on any current. It is directly proportional to absolute Temperature and is given by

$$v^2 = 4kTRf \tag{2.1}$$

The frequency spectrum for thermal noise is fairly constant across all frequencies.

1/f noise (flicker noise) is a narrow band noise that is primarily caused by manufacturing imperfections resulting in contamination of the transistors and resistors on the wafer. These imperfections in the wafer release carriers in a random fashion and so cause random noise in the current. This noise is usually confined to low frequencies and causes spikes in the current and is given by

$$i^2 = K1\frac{I^a}{f^b}f \tag{2.2}$$

K1 is a random factor that varies from case to case since the nature of manufacturing defects are random. 1/f noise occurs only when there is DC current in a device.

The sensor must minimize the affects of thermal and 1/f noise.

2.3 Signal Modulation

Signal modulation is the process of shifting a signal from its current frequency to another. This is accomplished by multiplication of two signals.

$$(Acos\omega t) \times (Bcos\alpha t) = \frac{A \times B}{2}[cos(\omega + \alpha) + cos(\omega - \alpha)] \tag{2.3}$$

Looking at a series expansion of a square wave of frequency ω, one can see that a square wave is made of a cos of frequency ω plus all of its odd harmonics.

$$Squarewave(\omega) = \frac{1}{2} + \frac{2}{\Pi}[cos(\omega t) - \frac{1}{3}cos(3\omega t) + \frac{1}{5}cos(5\omega t) - \frac{1}{7}cos(7\omega t) + \frac{1}{9}cos(9\omega t) - ....] \tag{2.4}$$

Multiplying a signal given by $cos\alpha t$ by a square wave we get

$$Acos(\alpha t)\times Squarewave(\omega) = (\frac{1}{2}\times Acos(\alpha t))+\frac{2}{\Pi}[\frac{A}{2}[cos((\omega+\alpha)t)+cos((\omega-\alpha)t)]...$$
$$-\frac{A}{6}[cos((3\omega+\alpha)t)+cos((3\omega-\alpha)t)]+\frac{A}{10}[cos((5\omega+\alpha)t)+cos((5\omega-\alpha)t)]...$$
$$-\frac{A}{14}[cos((7\omega+\alpha)t)+cos((7\omega-\alpha)t)]+\frac{A}{18}[cos((9\omega+\alpha)t)+cos((9\omega-\alpha)t)]-....] \quad (2.5)$$

The result is a signal at $cos(\omega+\alpha)$ and at $cos(\omega-\alpha)$ and all its harmonics. Modulating a signal by a square wave is the prefered method of modulating a signal because its easier to generate a square wave accurately then a sine wave.

2.4 Chopper stabilization

Chopper stabilization is a technique for reducing low frequency (1/f) noise that has been in use for a number of decades. It works by modulating the desired signal to a frequency above the frequencies where 1/f noise occurs. There the signal is amplified at that higher frequency and then it is modulated back down to the original frequency. Now the signal is amplified but the 1/f noise has been avoided. The modulating signal is usually a square wave and so when modulation occurs all the square wave's harmonics must be low pass filtered. The modulating frequency should be at least twice that of the signal being modulated.

Chopping is realized using MOS switches and so can suffer from transistor nonidealities. These nonidealities include clock feedthrough, charge injection, and MOS leakage current and can show up as voltage spikes.

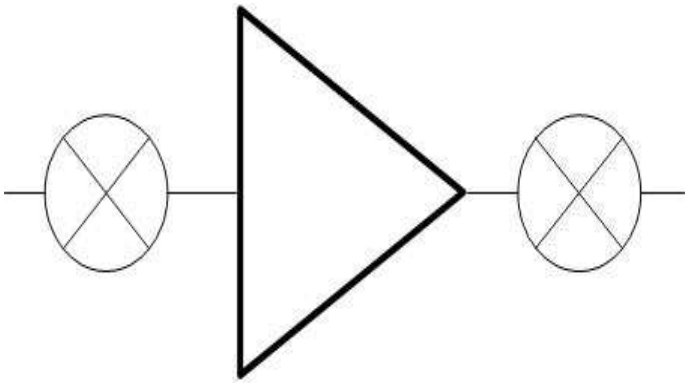

Figure 2.3: Chopper Stabiliztion

2.5 Lead input impedance

2.5.1 Wet Electrodes

For this design we need to model the impedance of the input electrodes. There are generally two types of electrode impedance models. Wet electrodes consist of two electrodes and an electrolyte. Each lead is modeled by the interface capacitace, Cinterface, in parallel with the charge transfer characteristics of the lead, Rinterface. Both of these are in series with the with the resistance of the electrolytic solution, Rsolution. The resistance of the solution is usually taken between the two electrodes and is a measure of the current that spreads throughout the solution. The electrolyte solution is designed to reduce the resistance of the the epidermis by increasing ion conductivity. Overtime these gels get dry and their impedances change. Also these gels cause skin irritation and attract bacteria so wet electrodes are not ideal for the long duration needed for heart variability sensing.

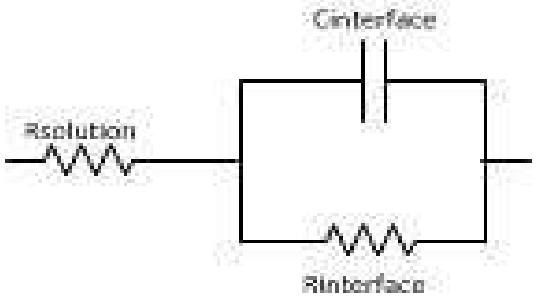

Figure 2.4: Wet electrode impedance model

2.5.2 Dry Electrodes

Dry electrodes attach directly to a patients skin without the need for an electrolyte. Standard dry electrodes have their issues as well. Hair underneath the electrode can change the resistance and friction with the skin can generate charge on the electrode. Sometimes electrodes are implanted in the skin however the body will form scar tissue around them and isolate them from the body. Some new flexible dry electrodes have been developed that use conductive foam to adapt to things like hair, reducing the effect of hair on impedance.

Chapter 3

Architecture

3.1 Chopper Stabilized Instrumentation Amplifier with embedded chopping

The instrumentation amplifier consists of a folded cascode differential amplifier with embedded output choppers. The amplifier is a differential-to-single ended amplifier that is fedback to the input. We want to boost the signal to a higher frequency when we amplify the signal so as to avoid amplifying low frequency noise and dc offset. So the signal is passed through an input differential chopper which modulates the signal by 1KHz which is well outside the input frequency band. The signal is amplified and the embedded chopper in the amplifier shifts the signal back down to the original frequency.

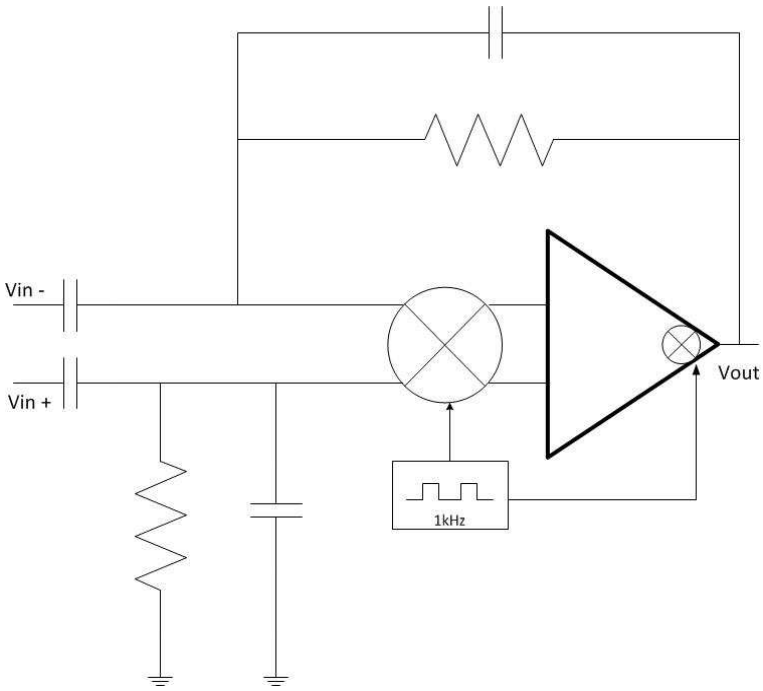

Figure 3.1: Instrumentation Amplifier

The higher order harmonics of the the square wave chopper are then low pass filtered out so that only the original amplified signal remains. One issue with this design is that the input chopper when combined with the capictance of the input transistor acts like a switch capacitor. This creates an undesirable path from the output of the amplifier through the feedback path through the input chopper to ground. Undesirable DC current flows out of amplifier to ground.

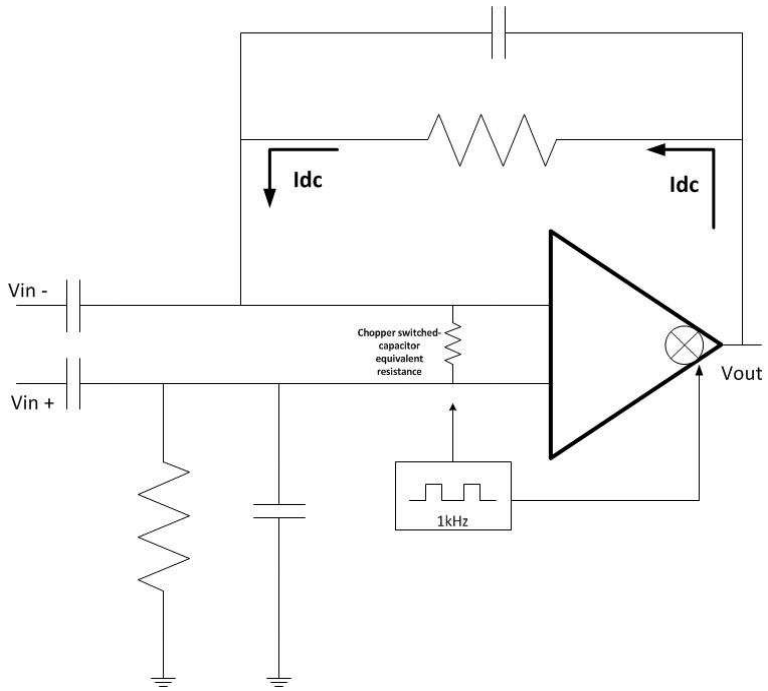

Figure 3.2: Undesirable DC current

To combat this a DC servo loop is used to provide the required DC current to ground and so that current is no longer being provided by the amplifier. The DC servo loop consists of a transconductance amplifier with a low pass filter at the output.

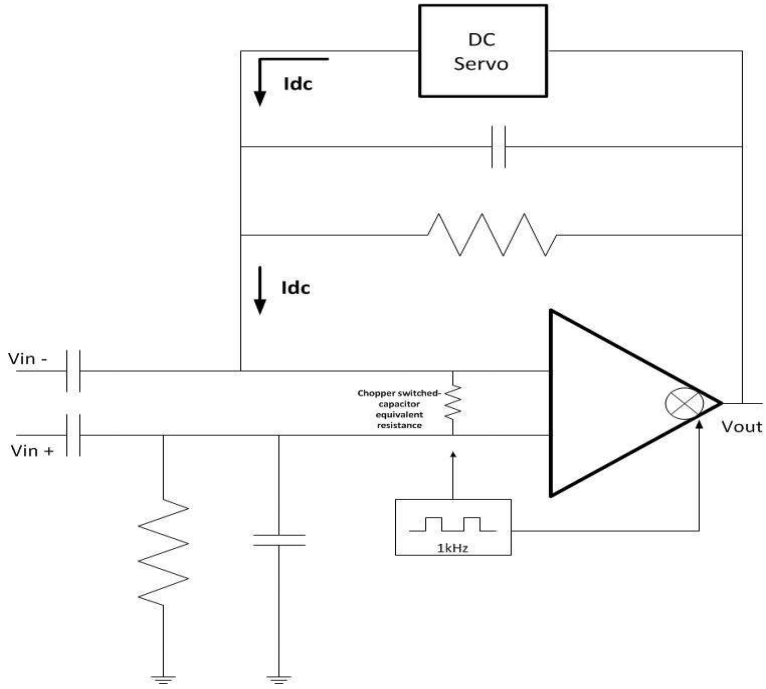

Figure 3.3: DC servo loop

3.2 d/dt peak detector

The peaks of the amplified signal are detected with a slope based peak detector. The idea is that the slope of the signal changes sign whenever a peak occurs. That change in slope can be detected and change the output value of the peak detector. The input signal into the detector is sampled and saved to a capacitor C1. On the next cycle the value on capacitor C1 is sampled by C3 while C1 samples the the input signal again. The difference between C1 and C3 is amplified and when the difference is positive as in cycle 2, that means the slope is positive and the NMOS transistor is ON and brings the output to ground. While the difference is negative like in cycle 11, the PMOS transistor is ON and the output is pulled to VDD. A rising edge at the output indicates a peak.

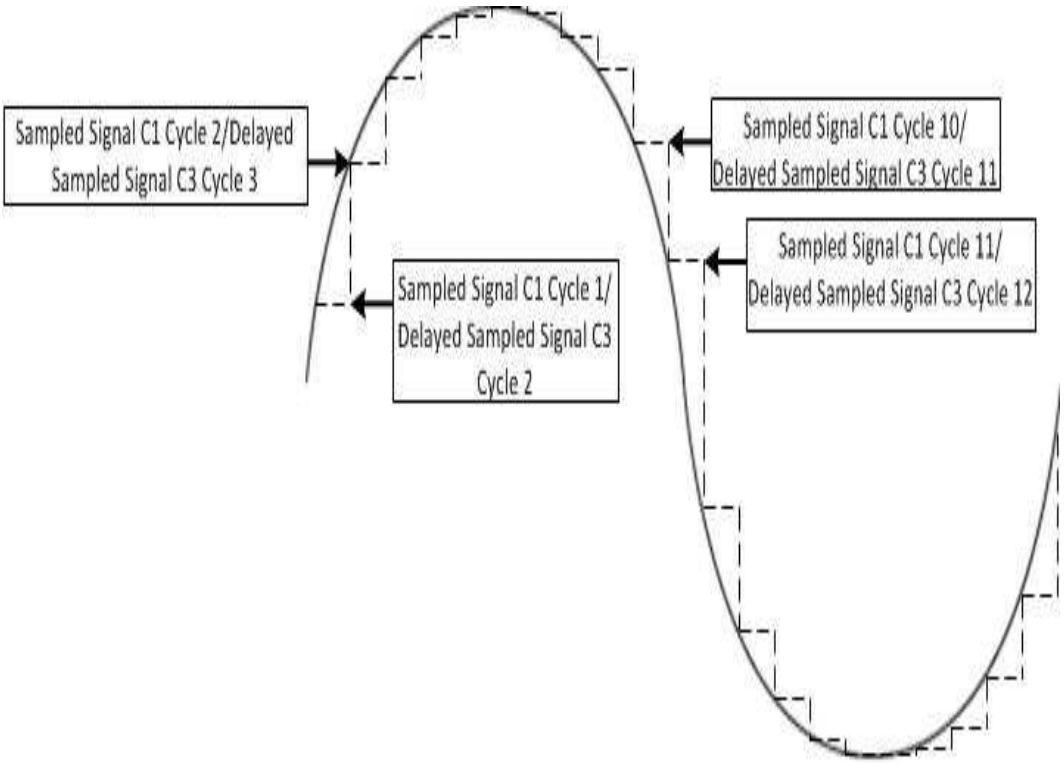

Figure 3.4: Peak Detector

Chapter 4

Design Specifics

4.1 Iamp design with embedded chopping

The operational amplifier is a folded cascode with embedded chopping and is designed with a TSMC 180nm process. VDD is set to 1.8V for this design while the amplifier is biased via feedback at 750mV. The **W/L** of the input transistors are kept wide to improve **gm**, while the **W/L** of the transistors in the transconductance stage were kept smaller to improve **ro**. DC current of the Op Amp was regulated primarily through the footer transistors (N1, N2, N3, N4, N5). N1, N2, N3, N4 were all sized the same so total current to ground in the folded cascode was equally distributed through each of the 4 transistors. The DC bias current of the each branch of the input stage is 86nA while the transconductance stage has bias currents of 83nA. The output stage consumes 239nA.

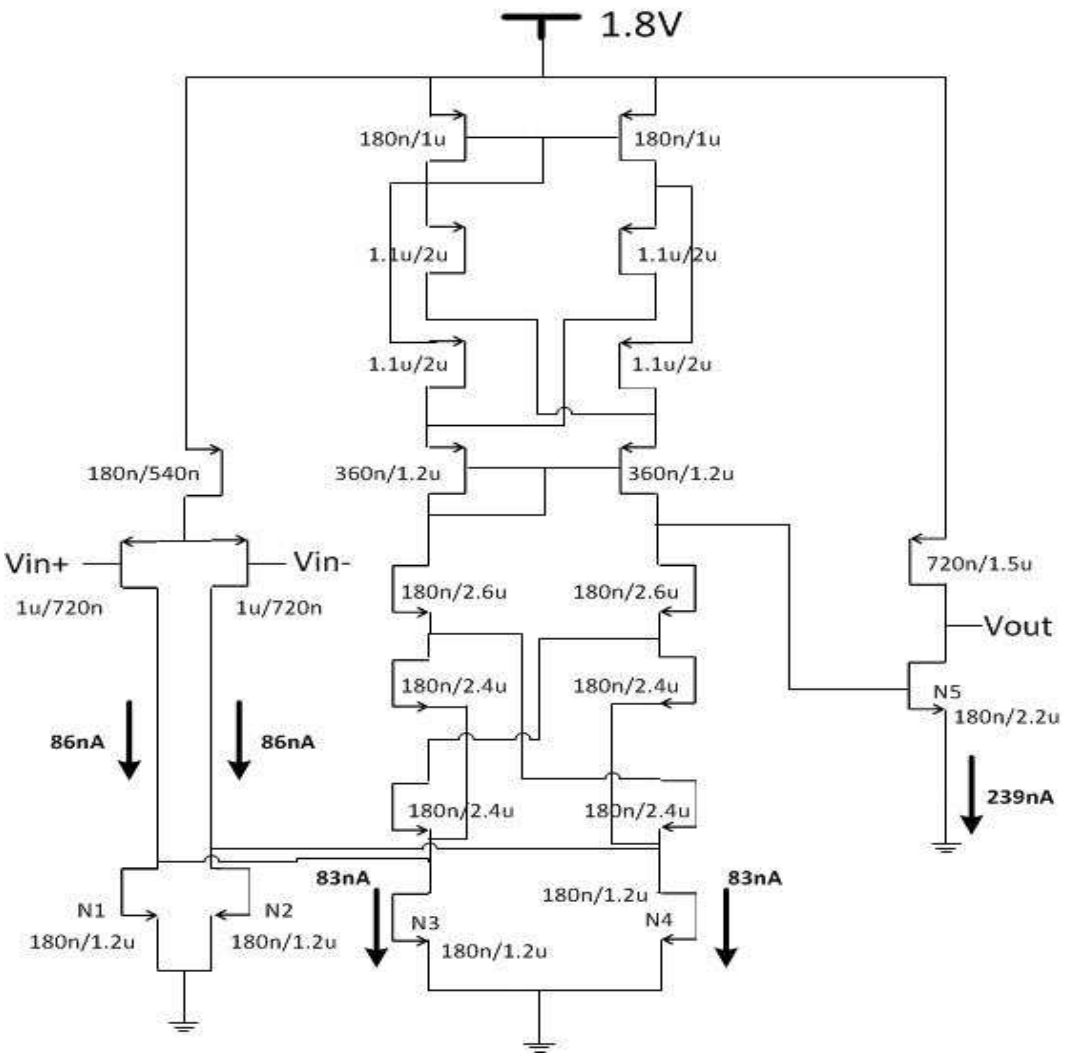

Figure 4.1: Operational Amplifier with embedded chopping

The embedded choppers work by directing the current from one branch to the other. The output choppers are square wave choppers where the clock toggles between VDD and GND with a 50 percent duty cycle.

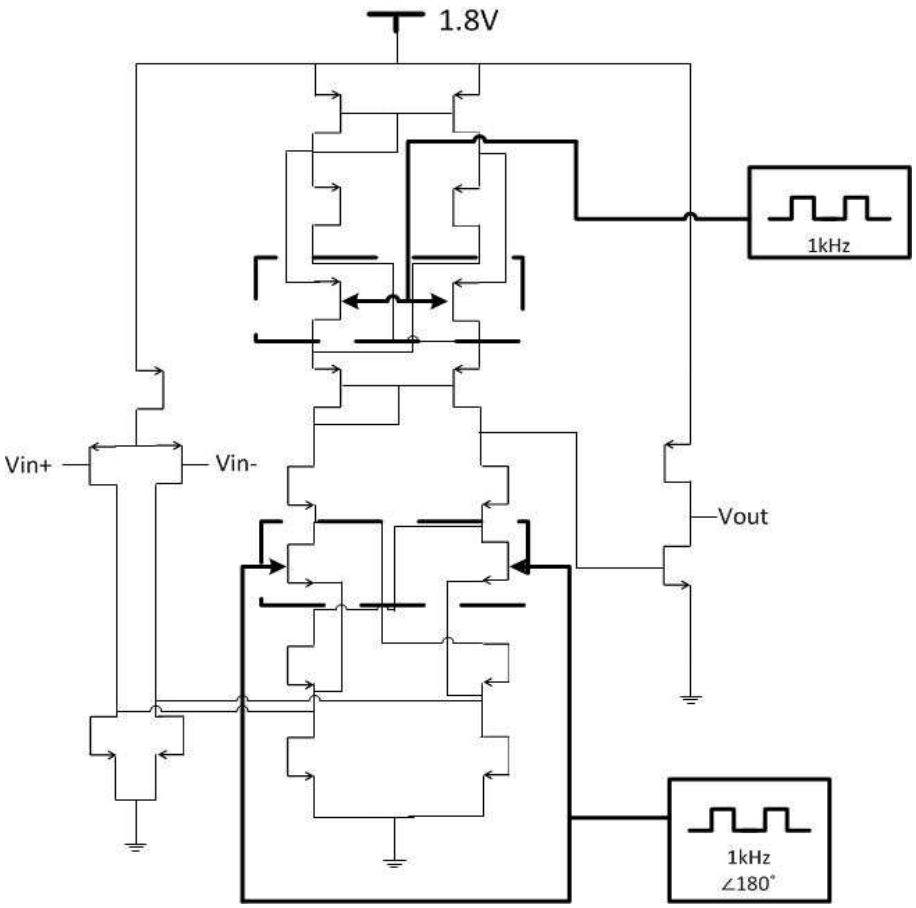

Figure 4.2: Output choppers with inside transistors ON

When the inside transistors of the output choppers are turned ON and the outside transistors are turned OFF, the current through the transconductance stage flows normally as seen above.

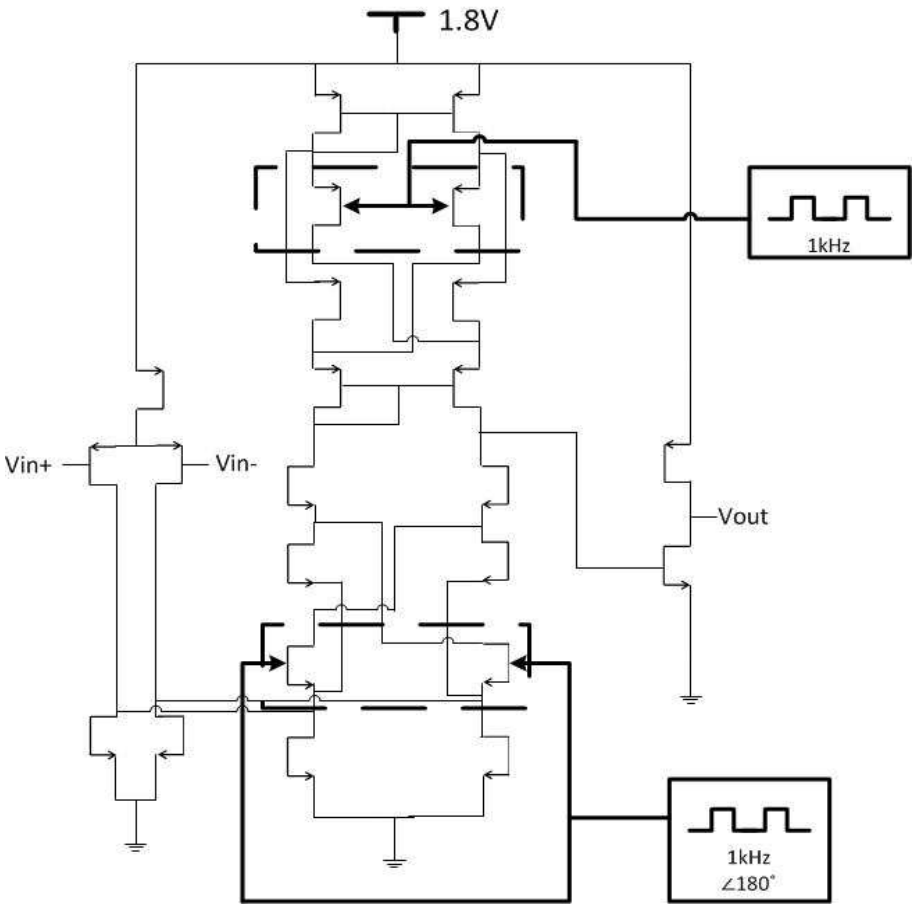

Figure 4.3: Output choppers with outside transistors ON

When the output transistors are turned ON and the input transistors are turned OFF the current through the transconductance stage is flipped. The clock toggles whether the inside transistors or the outside transistors are turned ON. This flipping of the current at the output performs the output chopping.

A symplified version of Iamp is shown

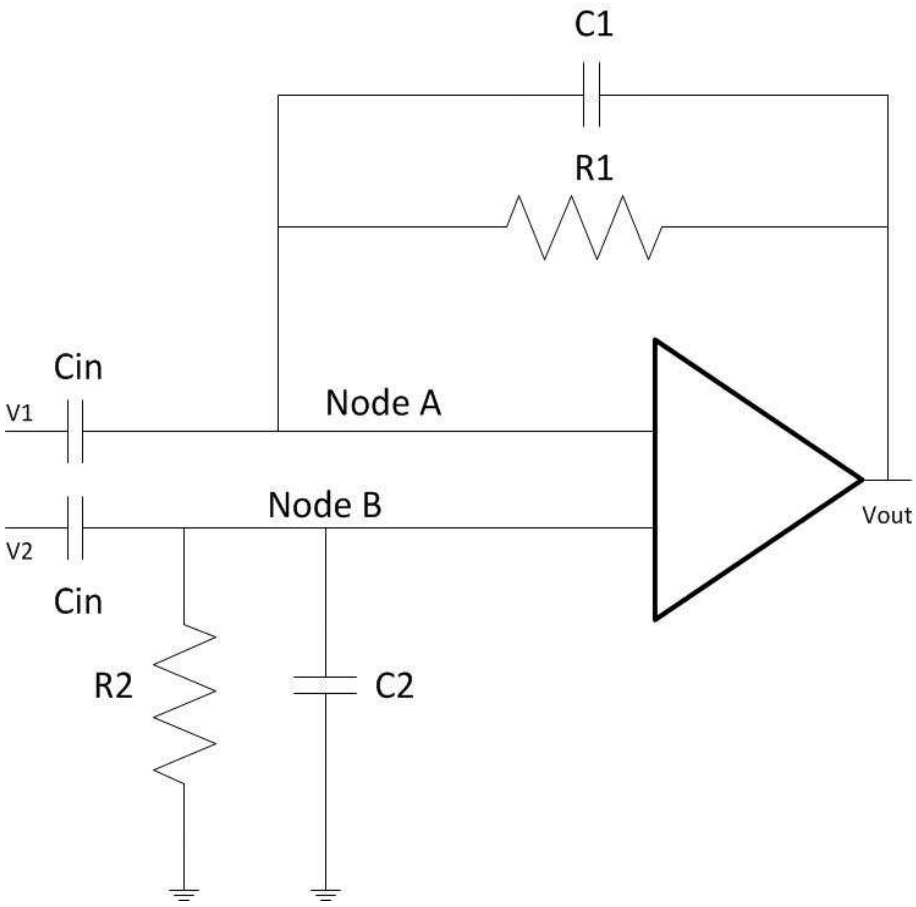

Figure 4.4: Instrumentation Amplifier

The nodal equation at Node A is given by

$$Va = \frac{Vout(j\omega C1R1 + 1) + V1(j\omega CinR1)}{j\omega C1R1 + 1 + j\omega CinR1} \tag{4.1}$$

The nodal equation at Node B is given by

$$Vb = \frac{V2(j\omega CinR2)}{1 + j\omega C2R2 + j\omega CinR2} \tag{4.2}$$

If C1=C2 and R1=R2 the Gain equation becomes

$$\frac{Vout}{V1 - V2} = \frac{-j\omega CinR1}{1 + j\omega C1R1} \tag{4.3}$$

So the gain is set by the ratio of Cin and C1. It is important to remember that Cin also sets the high pass corner where we want the high pass corner to be about 0.40Hz. Setting C1=C2 and R1=R2 also improves CMRR.

4.2 Input Differential Choppers

The input differential choppers consist of four transistors that perform square wave chopping. The differential input signal is multiplied by +1 and -1 meaning that the input is multiplied by all of the square waves harmonics. The chopping frequency is set to 1KHz, well outside the band of interest and high enough frequency to mitigate 1/f noise when amplifying. All four transistors are sized equally. As mentioned previously these switches when interacting with the gate capacitance of the input transistors acts like a switched-capacitor resistor and creates a path from the output of the amplifier to ground drawing 40fA.

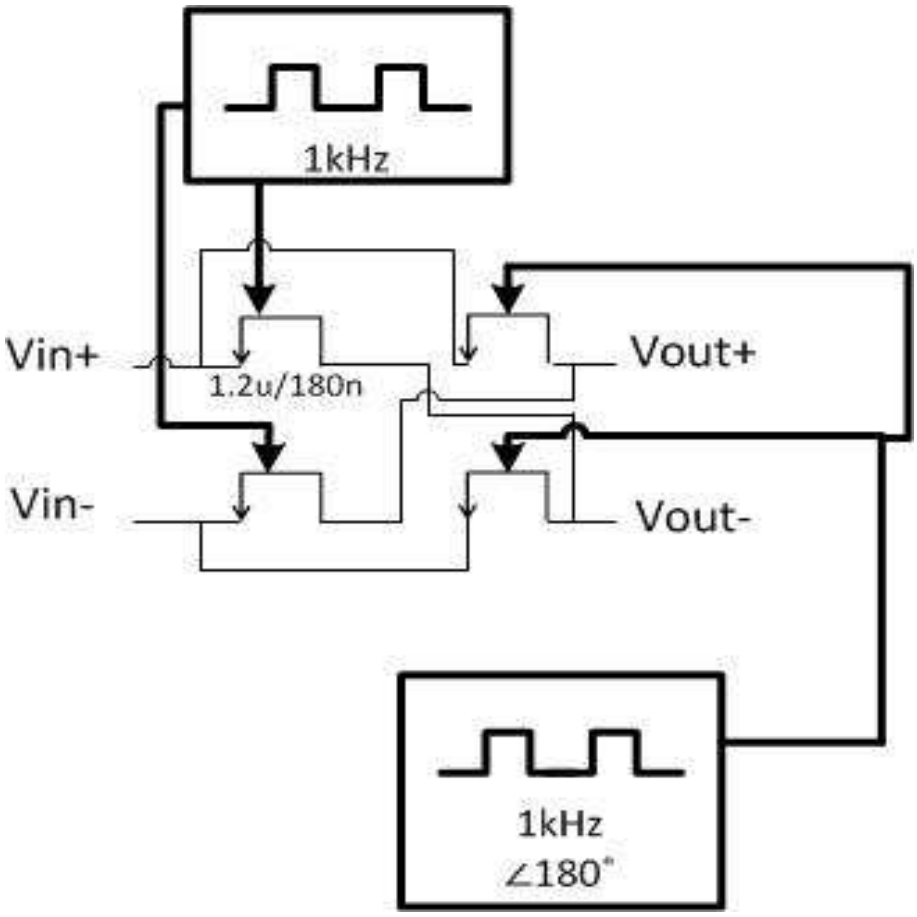

Figure 4.5: Input Differential Chopper

4.3 DC Servo Loop

The DC servo loop is used to compensate for the DC current flowing through the input chopper to ground. It was determined that this servo loop needs to provide 40fA of current. This is achieved by using a transconductance amplifier. A transconductance amplifier senses the input voltage and produces an output current. The circuit is shown below .

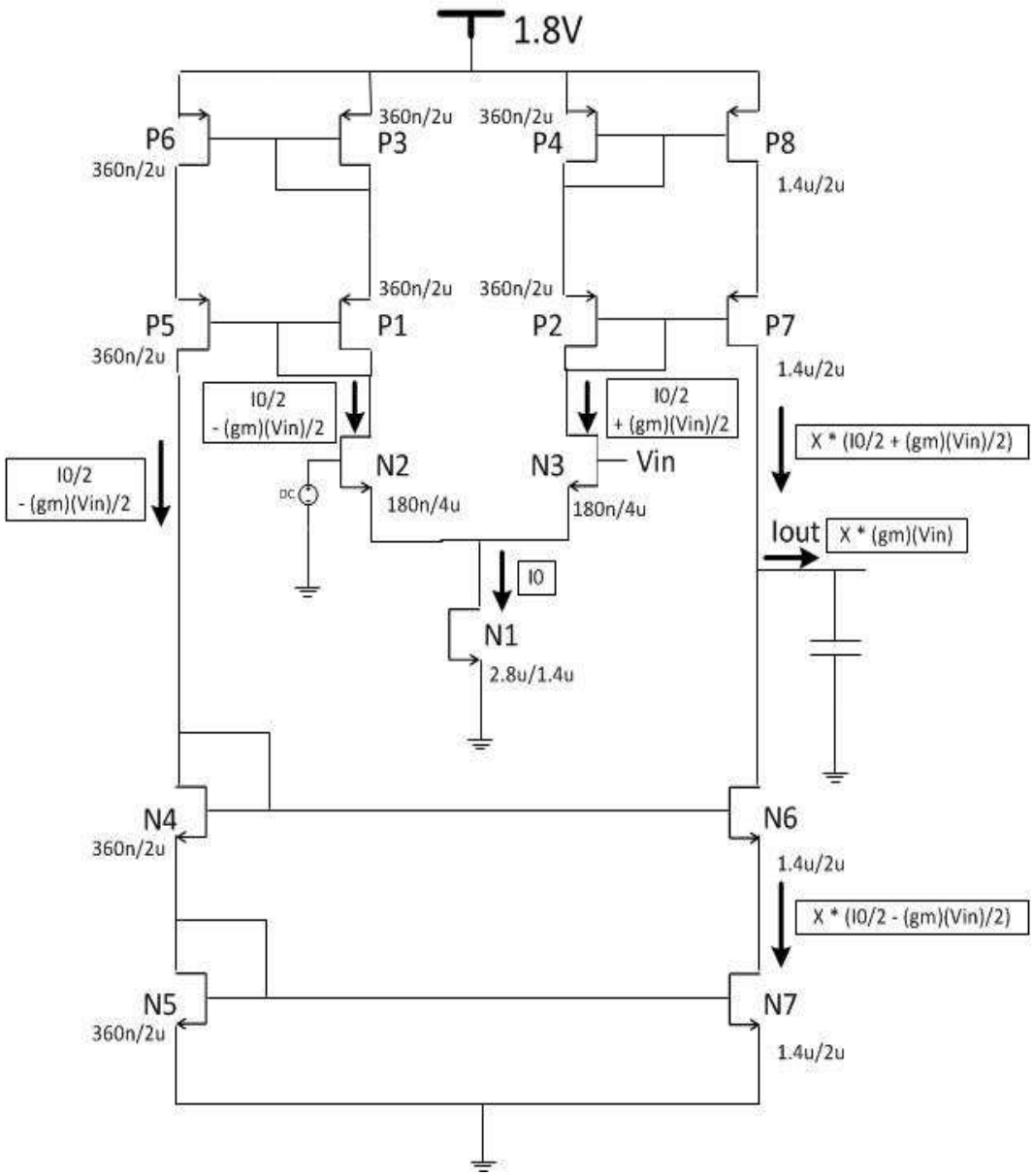

Figure 4.6: Transconductance Amplifier

The two input branches nominally have half the tail current $\frac{I0}{2}$ in both branches. For an input Vin, $\frac{I0}{2} + \frac{(gm)(Vin)}{2}$ will appear on one branch and $\frac{I0}{2} - \frac{(gm)(Vin)}{2}$ on the other branch. The current on the right branch is mirrored using P4 and P2 onto P8 and P7 with ratio X. The current on the left branch is mirrored using P3 and P1 onto P6 and P5. The current is then mirrored from N4 and N5 onto N6 and M7 with ratio X. Now the output branch has $X \times (\frac{I0}{2} + \frac{(gm)(Vin)}{2})$ through P6 and P7 and $X \times (\frac{I0}{2} - \frac{(gm)(Vin)}{2})$ through N6 and N7, therefore the output current delivered is

$$Iout = X \times (gm)(Vin) \tag{4.4}$$

Transistors are stacked at the output to improve the output impedance. This is important so that the servo loop delivers a constant current.

$$Rout = (roN6[1{+}gmN6roN7]{+}roN7) \parallel (roP7[1{+}gmP7roP6]{+}roP6) \tag{4.5}$$

Since only DC is desired out of the transconductance amplifier the output is low pass filtered. The total output current delivered is 38.7907fA. This leaves the the main amplifier delivering only 1.18fA.

4.4 Low Pass Filter Design

This filter is a two pole low pass filter. It is used to filter out the harmonics from chopping leaving only the original frequency band.

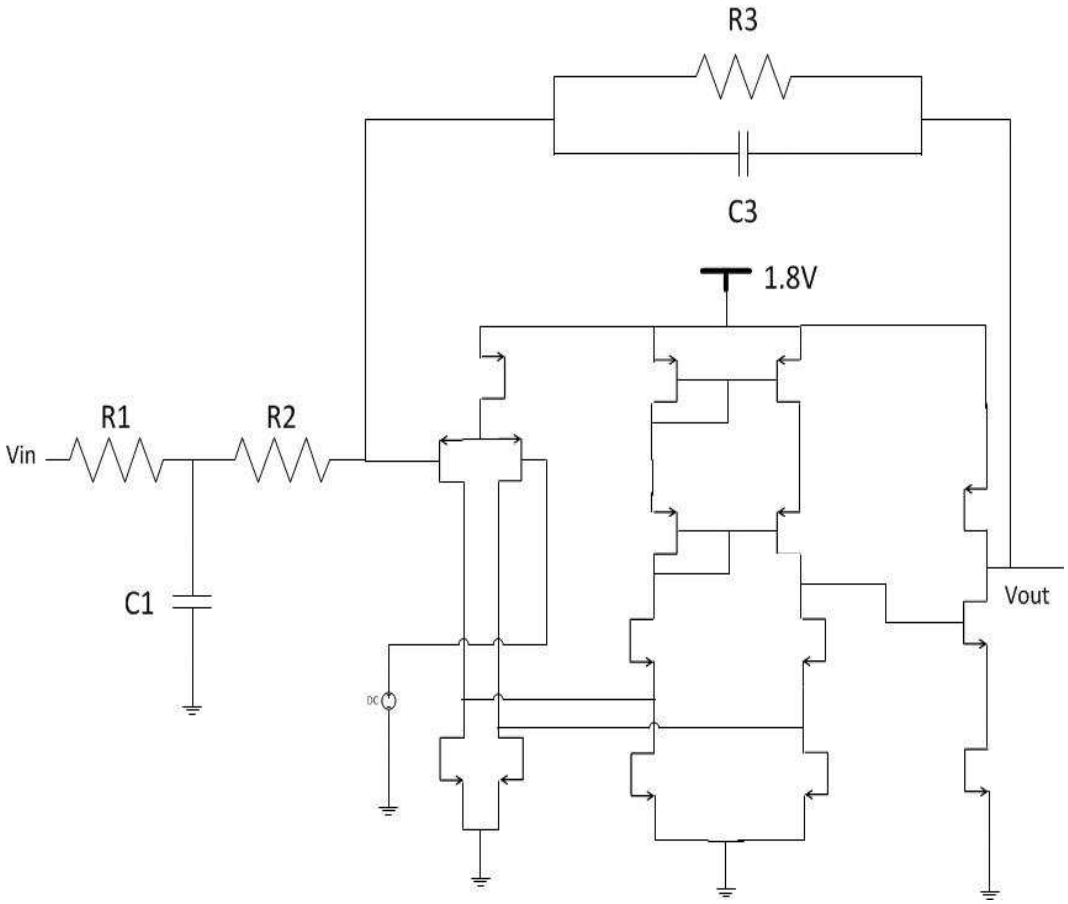

Figure 4.7: Low Pass Filter Design

4.5 d/dt peak detector design

The signal coming from the Iamp is sampled at 1KHz. The higher the sampling frequency, the more accurate the peak detection. A transmission gate is used to sample the signal and save it onto capacitor C1. The clock toggles between VDD and 0. On the low phase of the clock cycle, C2 will sample whats on C1. On the next high phase of the clock that sampled signal that was on C2 will be on C3 while

C1 will have a new sample of the signal.

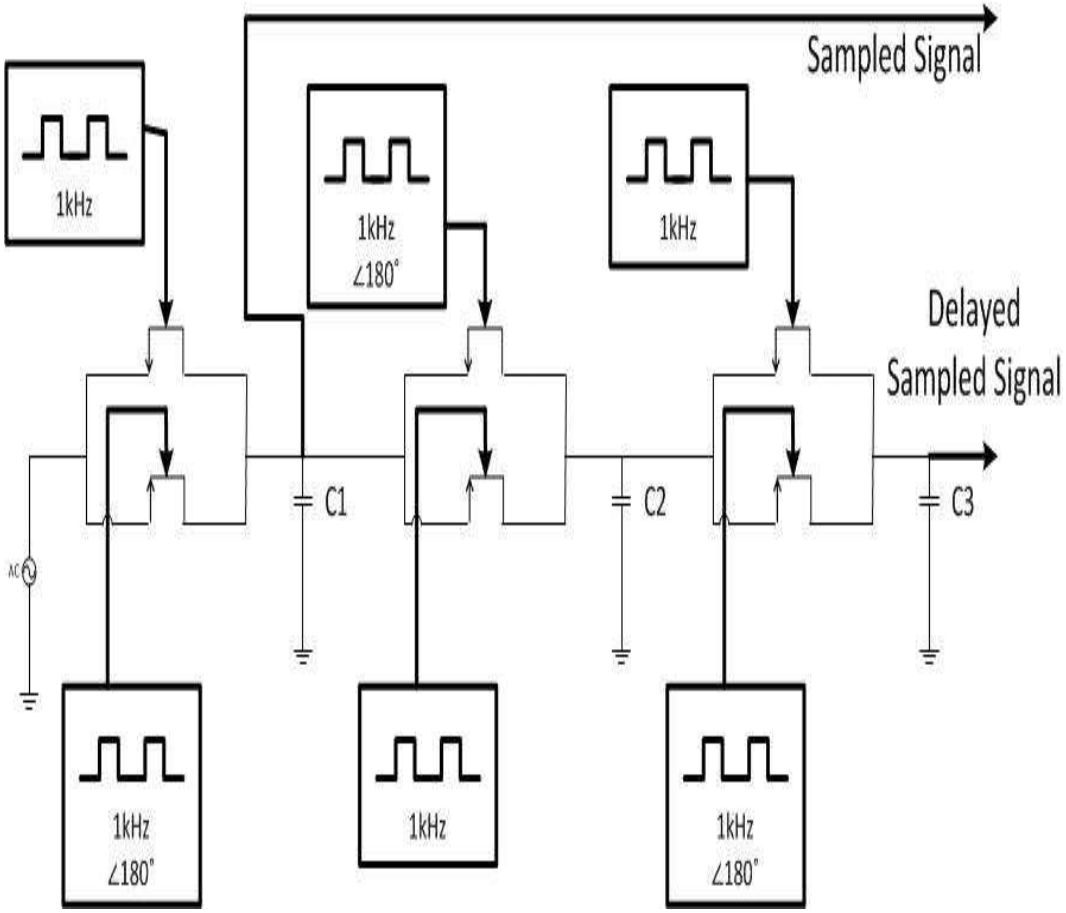

Figure 4.8: Peak Detector Sampler

The difference between the sampled signal and the delayed sampled signal is found with a difference amplifier.

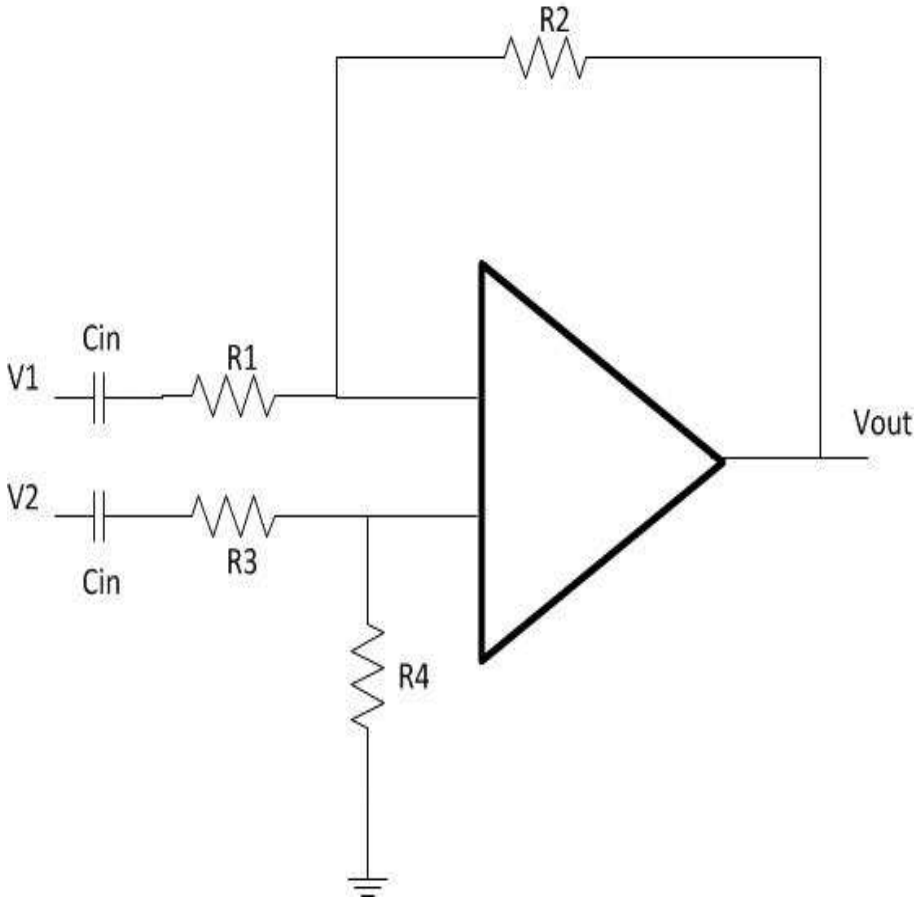

Figure 4.9: Difference Amplifier

Vout is the difference between V1 and V2 and is given by

$$Vout = \frac{R2}{R1}\frac{1+\frac{R1}{R2}}{1+\frac{R3}{R4}}V2 - \frac{R2}{R1}V1 \tag{4.6}$$

If R1=R3 and R2=R4 then difference amplifier becomes

$$Vout = \frac{R2}{R1}(V2 - V1) \tag{4.7}$$

The output of the difference amplifier drives an inverter and the output capacitor will indicate a peak on a rising edge.

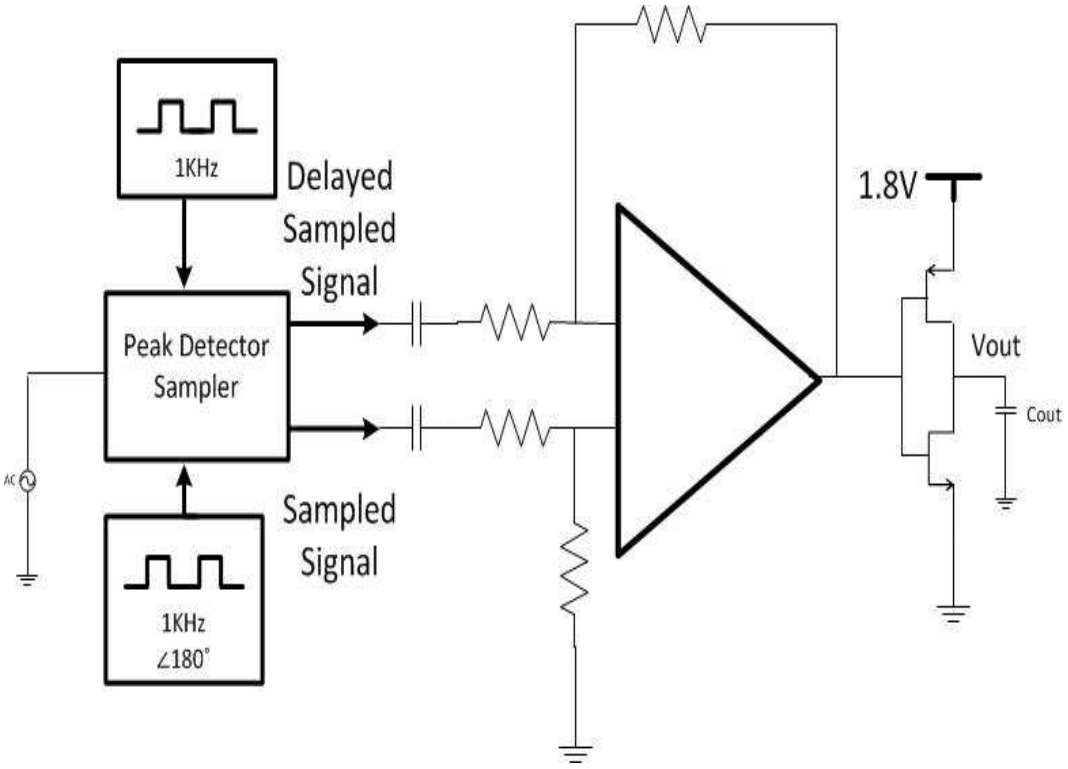

Figure 4.10: Peak Detector

4.6 Input electrode resistance modeling

The input resistance of the electrodes are modeled as a capacitor in parallel with a resistance. As part of the specification, input electrode imbalance needs to be tested. 620kohms was placed in parallel with 4.7nF capacitor on one lead while on the other lead 51kohms was in parallel with 47nF. The desired Gain-Bandwidth of the Iamp was maintaned. The electrode impedances were swapped and Gain-Bandwidth was still maintained.

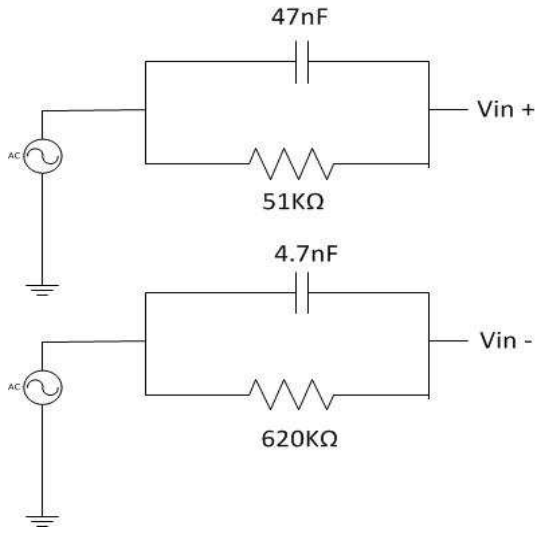

Figure 4.11: Input electrode resistance model

Chapter 5

Simulation Results

5.1 Gain of Iamp

The Gain of the front-end Iamp is 20dB and is shown below. The 3dB frequency of the high pass corner is at 0.37Hz

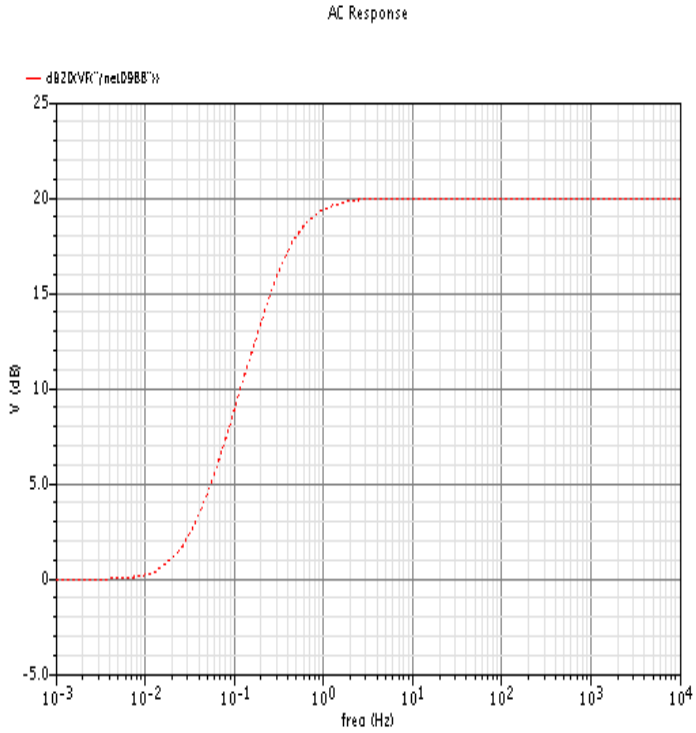

Figure 5.1: Instrumentation Amplifier Gain

5.2 Gain of Iamp and Low Pass Filter

The Gain after the Low Pass Filter is added is 13.86dB.

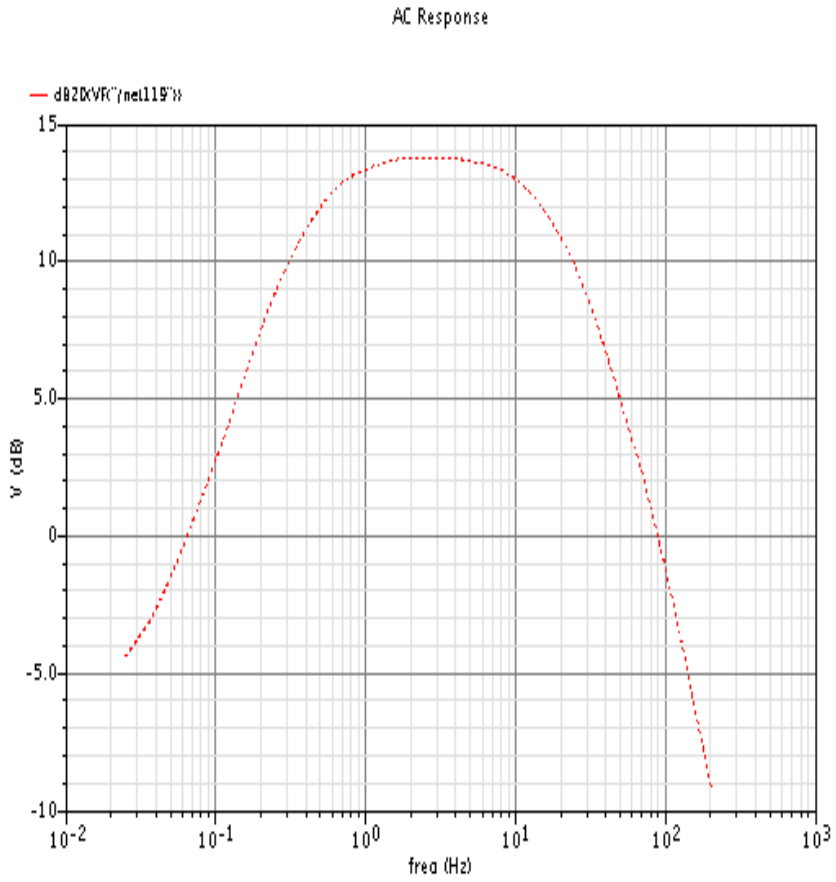

Figure 5.2: Instrumentation Amplifier + Low Pass Filter Gain

5.3 CMRR of Iamp plus low pass filter

The Common mode Gain ranges between -13dB and -53dB therefore CMRR ranges between 27dB and 67dB.

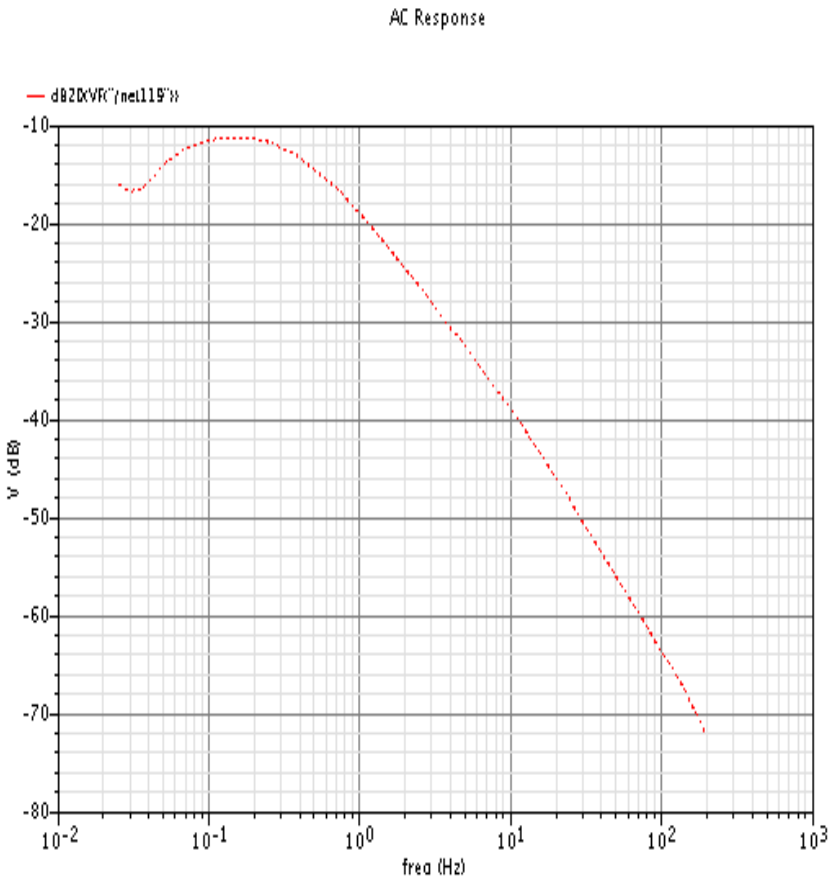

Figure 5.3: Instrumentation Amplifier + Low Pass Filter CMRR

5.4 Noise simulation of Iamp

Simulations show the maximum value to be $28n\frac{v^2}{sqrt2Hz}$

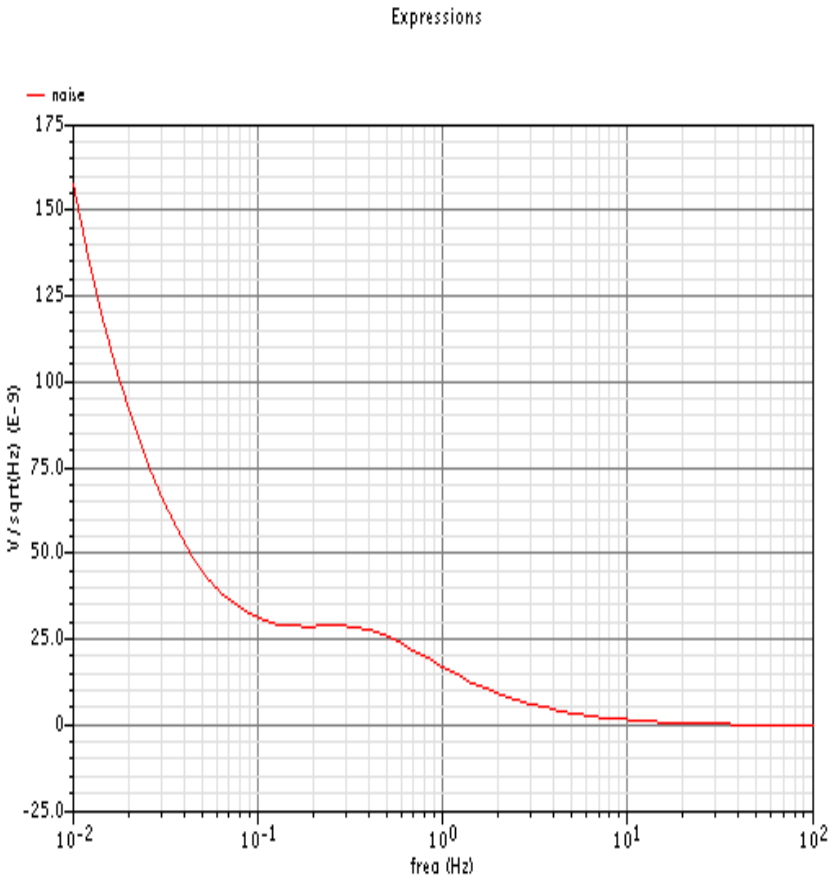

Figure 5.4: Noise of Iamp + Low Pass Filter

5.5 Iamp plus Low Pass Filter Input Dynamic Range

The Input dynamic range was tested by setting the input DC bias to 850mV and 650mV and making sure parameters were still met.

5.5.1 Iamp plus Low Pass Filter Input Dynamic Range 850mV bias

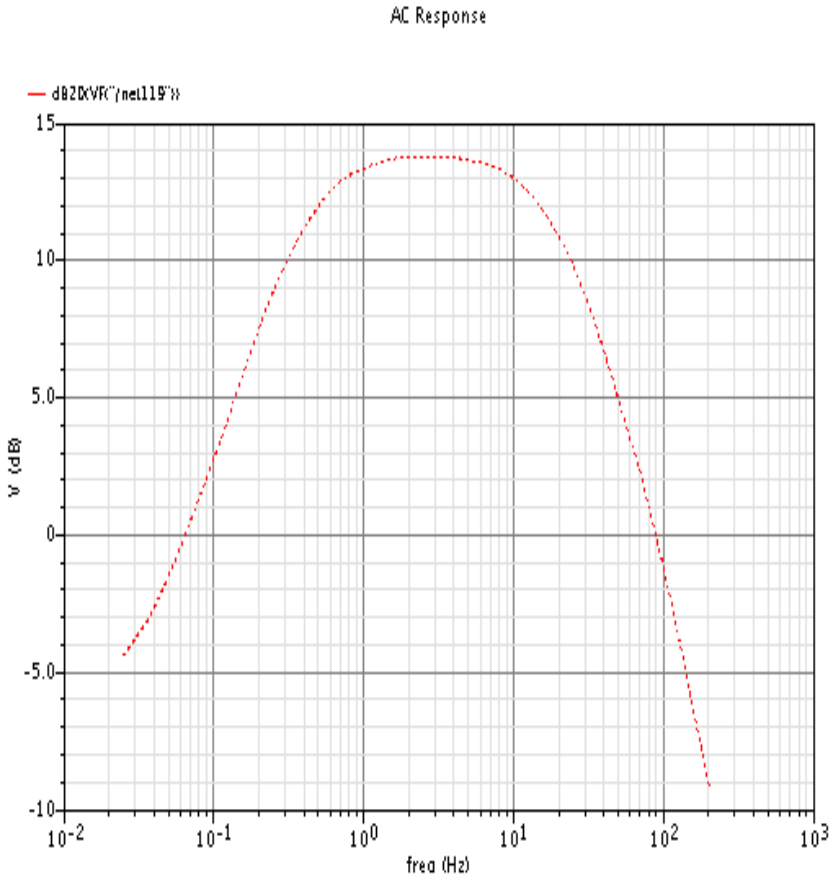

Figure 5.5: Differential Gain with 850mV bias

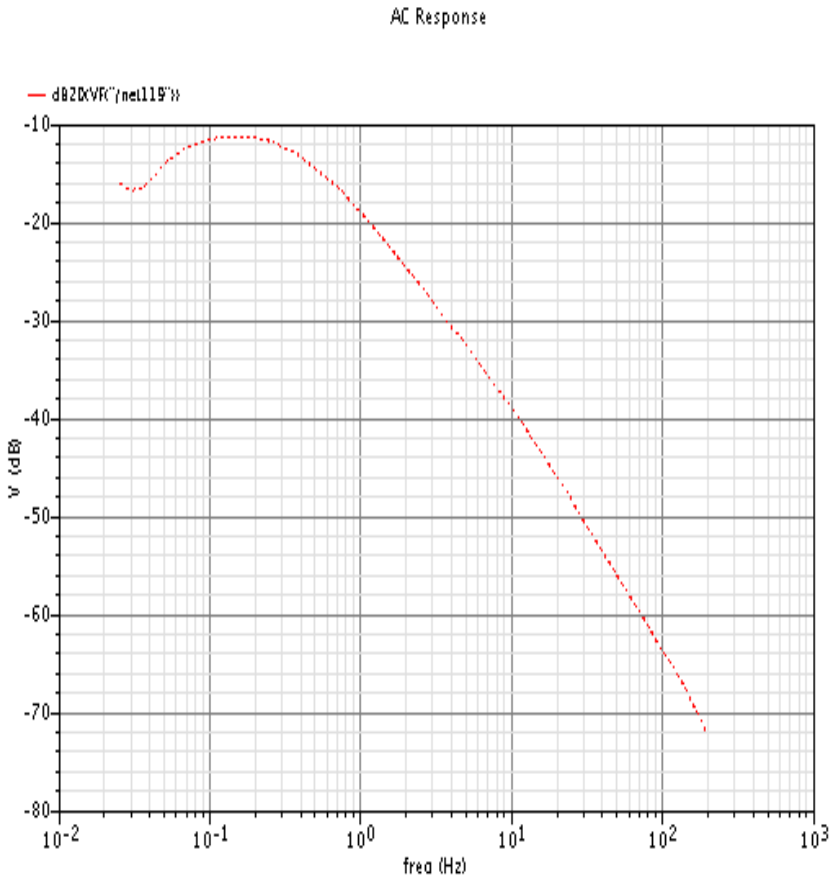

Figure 5.6: Common-mode Gain with 850mV bias

5.5.2 Iamp plus Low Pass Filter Input Dynamic Range 650mV bias

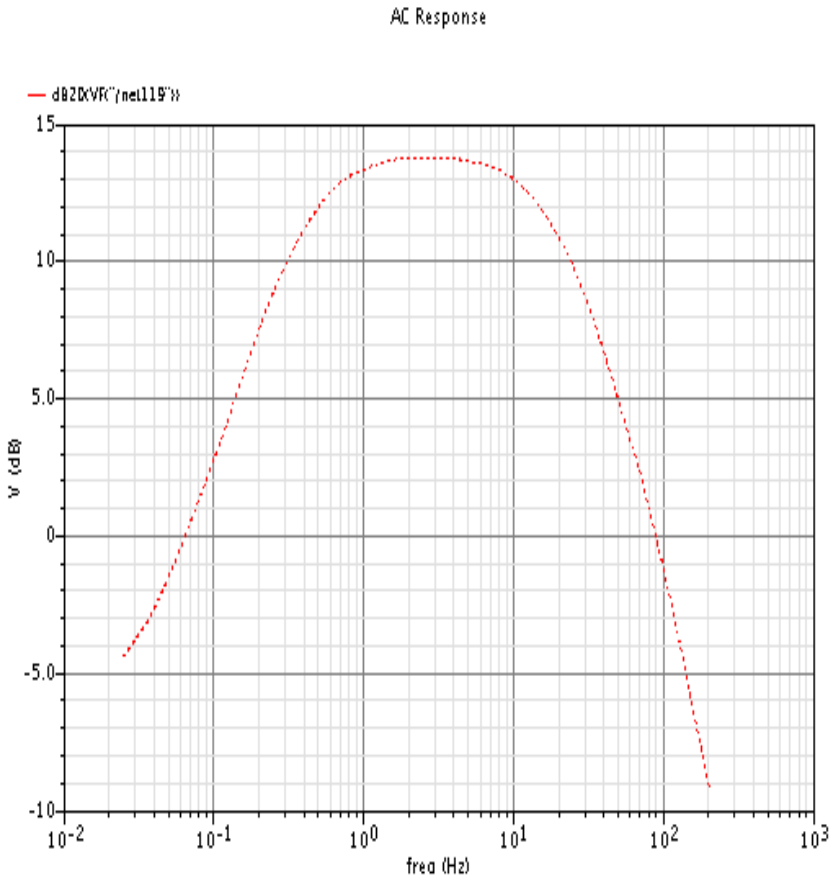

Figure 5.7: Differential Gain with 650mV bias

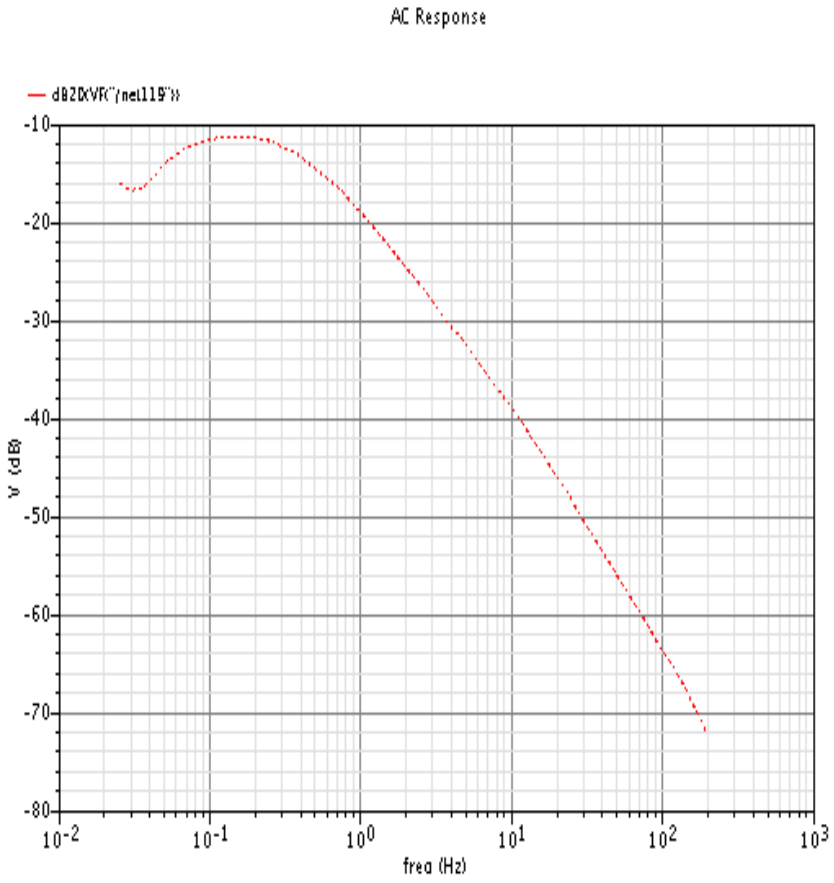

Figure 5.8: Common-mode Gain with 650mV bias

5.6 Iamp input impedance

Input current was measured with a 1mV 10Hz test AC voltage on the feedback input

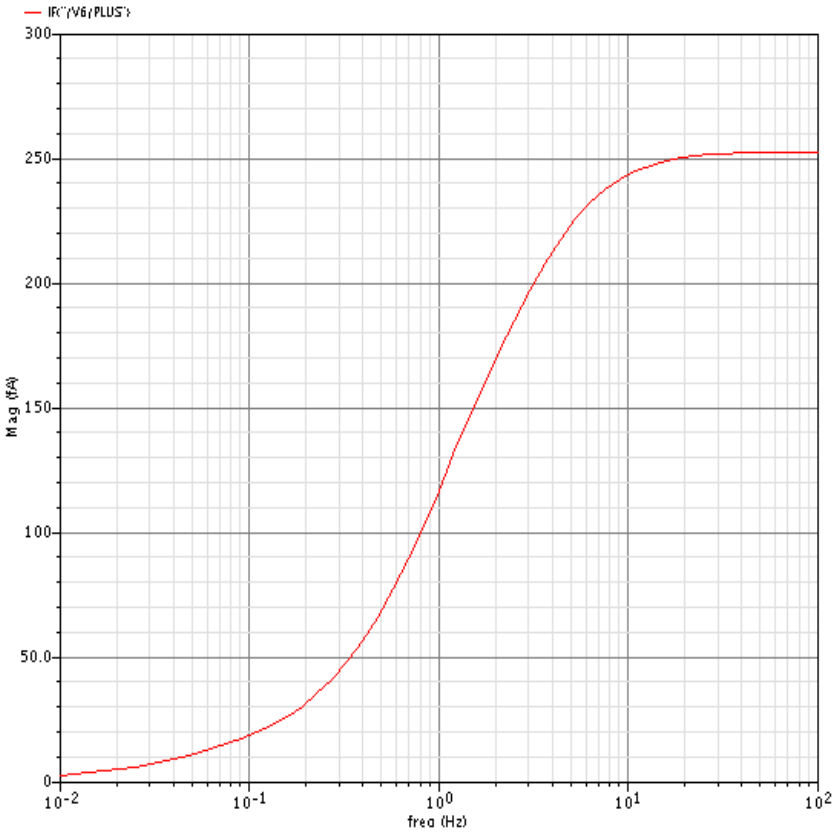

Figure 5.9: Input Impedance for the feedback input

It is seen here that the input current is approx 240fA giving an input resistance on the feedback lead of 4G ohms

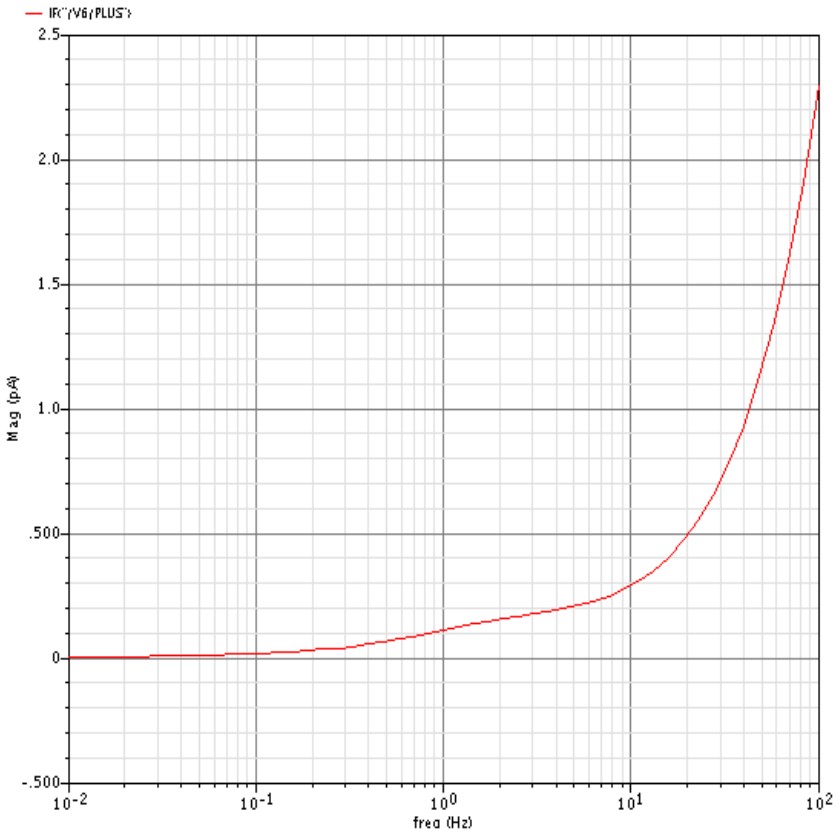

Figure 5.10: Input Impedance for the non-feedback input

With the same test voltage on the non-feedback lead the current is 299fA making the input impedance 3.3G ohms. Current begins to rise rapidly as frequency increases. However at 40Hz, the current is under 1pA meaning that resistance is above 1G ohms, therefore the input of this Iamp is well beyond the 5M ohms required.

5.7 Transient analysis of peak detector

A 40Hz 10mV sine wave input was used to test the peak detector. It is being sampled at 1KHz. The difference drives the output signal as described previously.

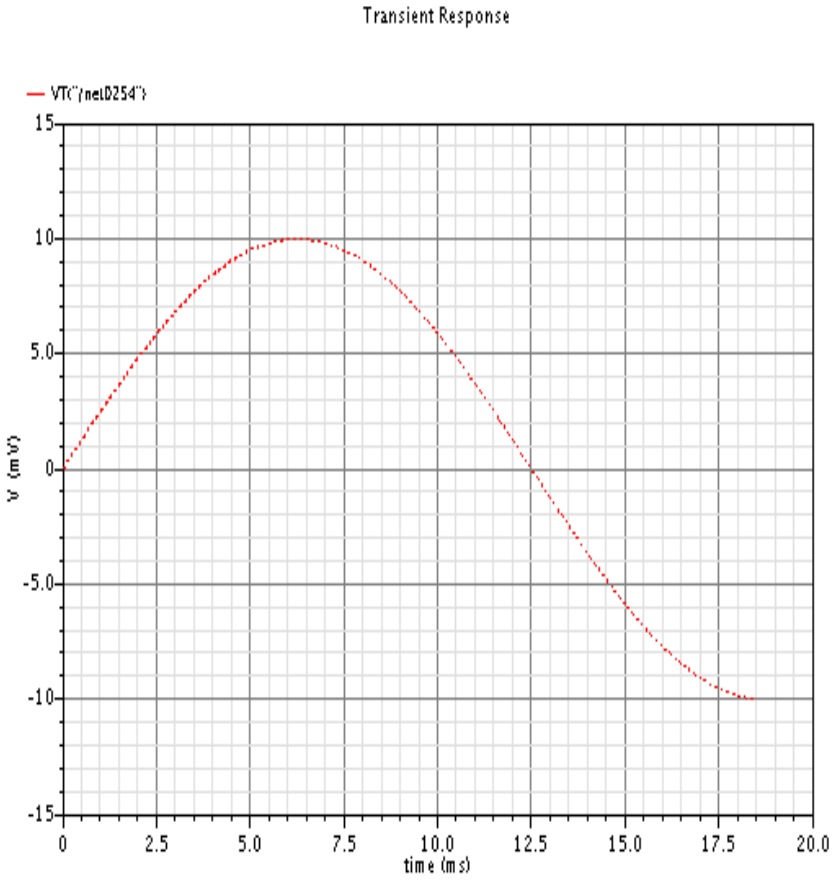

Figure 5.11: Input to Peak Detector

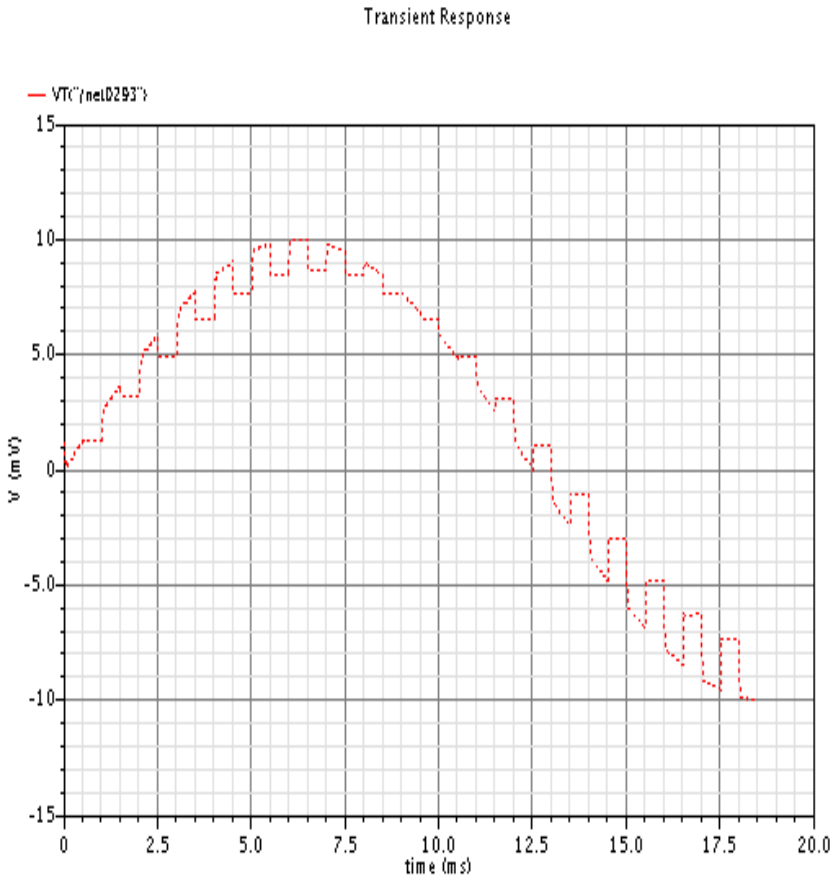

Figure 5.12: Sampled input of Peak Detector

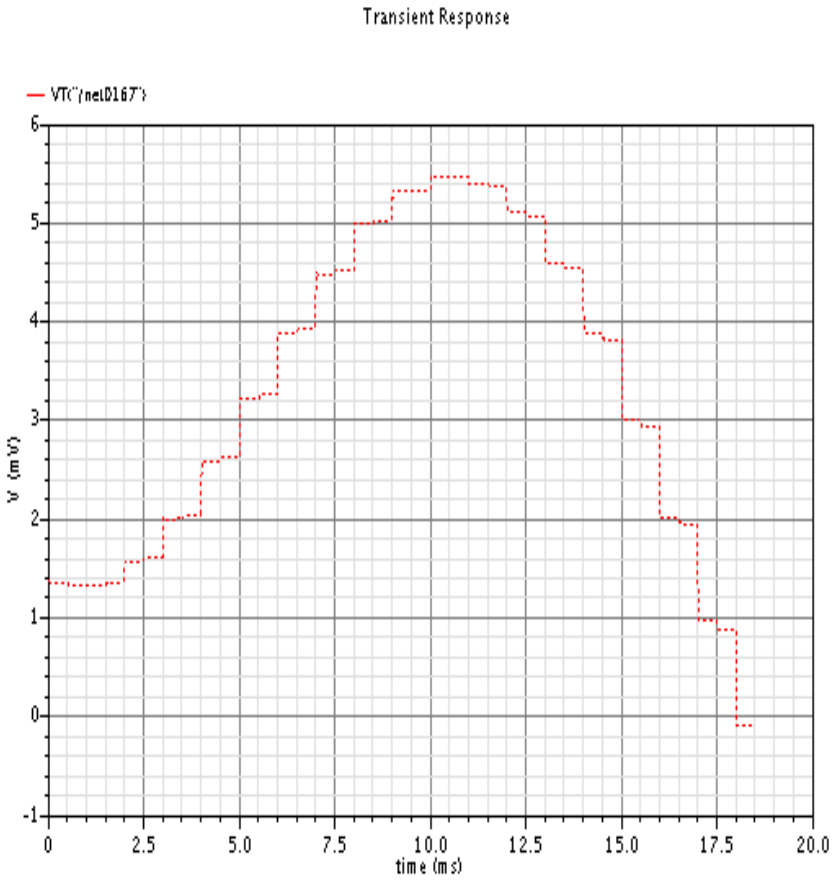

Figure 5.13: Delayed Sampled input of Peak Detector

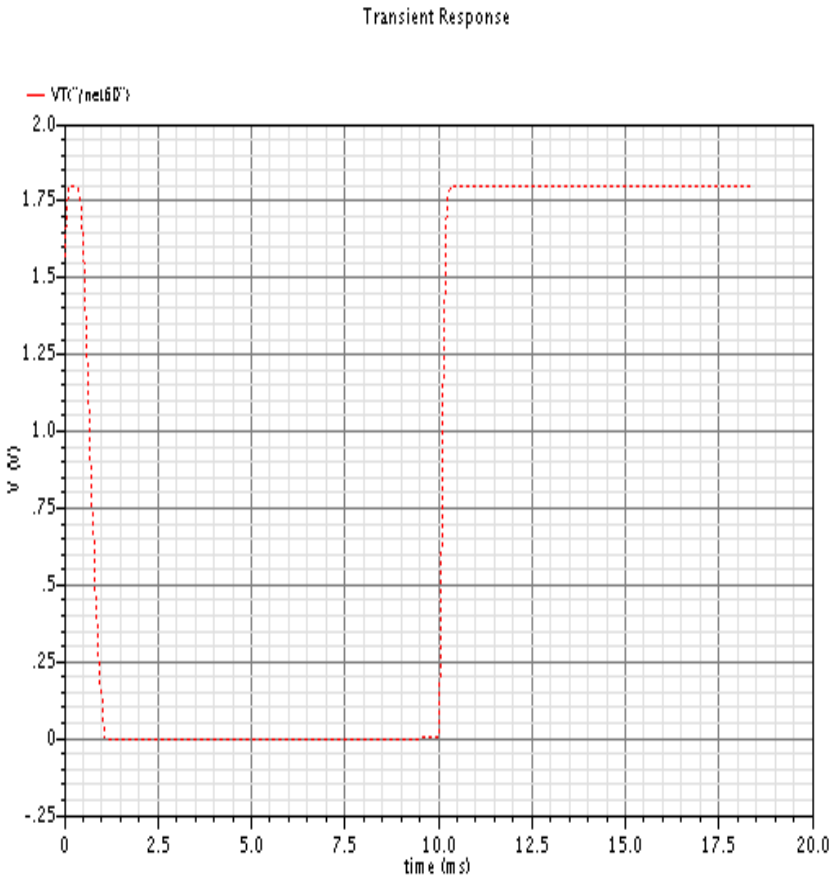

Figure 5.14: Output of Peak Detector

The sampled signal, the delayed sampled signal, and the output of the peak detector are shown. A rising edge at the peak detector output indicates a peak. There is a 4ms delay between the peak of the input and when the rising edge of the peak detector is seen. This is due the fact that a delayed sample is needed to take the difference which delays the output and also there is some degradation in the voltage of the delayed sample. This means that the crossover point where the delayed sample is at a higher voltage than the original sample and the peak detector output changes value is further delayed.

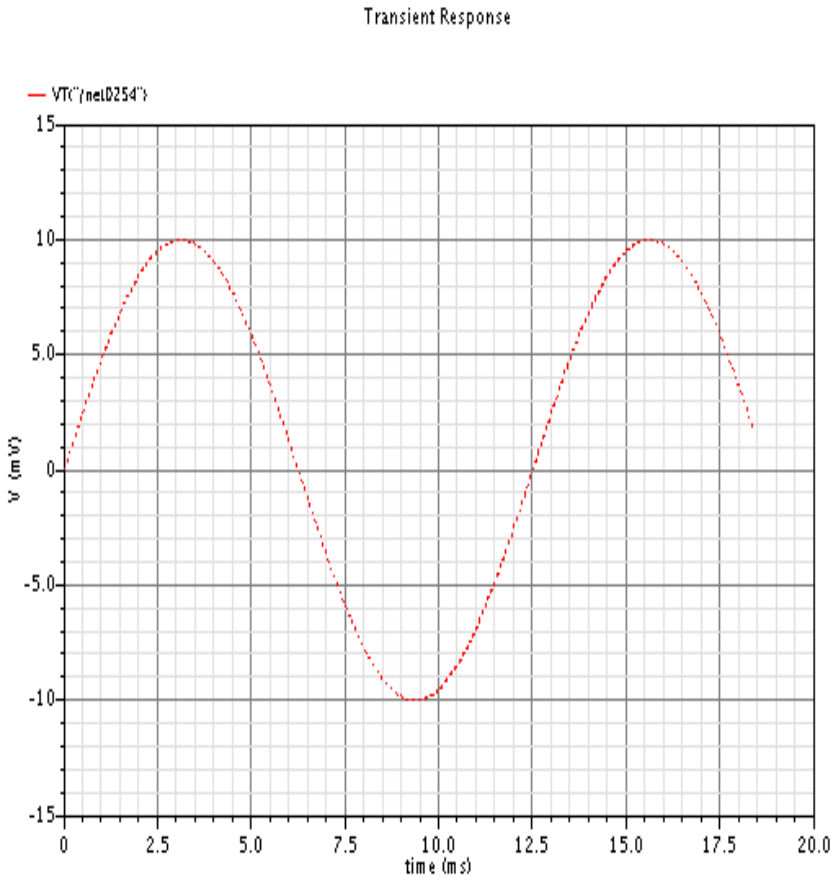

Figure 5.15: 80Hz Input to Peak Detector

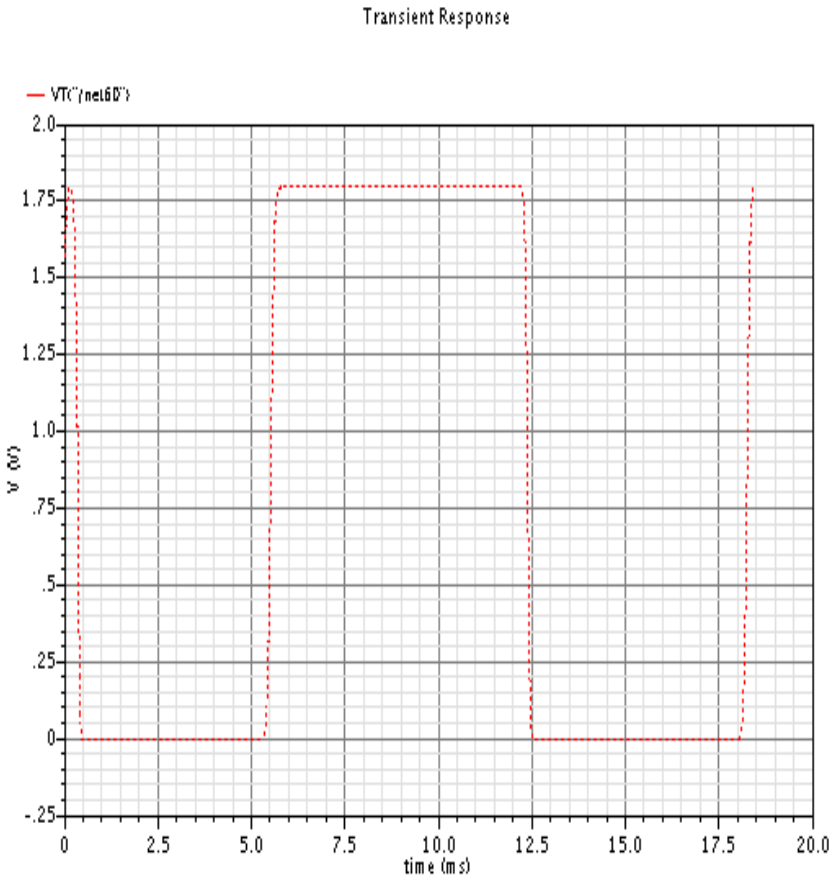

Figure 5.16: Output of Peak Detector for 80Hz

An 80Hz input signal is also shown above with the output of the peak detector.

5.8 DC power consumption

The Instrumentation Amiplifier with Low Pass Filter consumes 2.133uA of current making its power consumption 3.834uW.

The total current consumed including the peak detector is 5.338uA making the total power consumption 9.60uW

Chapter 6

Conclusion

This project demonstrated a design of a low power, low noise analog front end for a heart variability sensor. A chopper stabilized Instrumentation Amplifier was used to amplify the signal while reducing 1/f noise. To find signal peaks a peak detector is used that looks for changes in the sign of the slope of the signal. Also the electrode impedance was modeled and the effect of impedance imbalance was checked. The instrumentation amplifier with low pass filter was low noise and all the components had less than 10uW DC power consumption.

In the future, circuits will have to be developed to generate voltage references and clocks. One advantage with this design is that only one frequency needs to be generated (1KHz). Also it is desirable to reduce the amount of the delay between when the signal peak occurs and when it is detected by the peak detector. There is room for improvement in DC power consumption. One way is to further reduce VDD to under 1V. Nonidealities due to chopping can be reduced by considering nested chopping.

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